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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,589	12/15/2000	Steven Teig	SPLX:P0014	3540

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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/739,589	Applicant(s) TEIG ET AL.	
	Examiner A. M. Thompson	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 Sept 03 thru 15 March 04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28,30-52 and 54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28,30-52 and 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/20/03; 10/10/03; 12/12/2003*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' amendment to 09/739,589 has been examined. Claims 28, 52, 54 are amended. Claims 29, 53, 55, and 56 are cancelled. Claims 28, 30-52 and 54 are pending.

1. Upon reconsideration, new grounds of rejection are entered in the instant application. Accordingly, this second non-final action on the merits issues.

Claim Objections

2. Claims 34, 35, 50, 51, 52, 54 are objected to because of the following informalities: Pursuant to claims 34 and 35, it contains steps a) and b), and steps a), b) and c), respectively, which are duplicated in claim 28; claims 34 and 35 require their own unique lettered steps. Pursuant to claim 50, at step d), line 1, delete "particular"; at line 3, change "graphs are" to - -graph is- -; at line 4, change "shortest" to - -a short- -. Pursuant to claim 51, at line 3, change "graphs" to - -graph- -; change "shortest" to - -a short- -; additionally, at line 5, "the first predetermined number" lacks sufficient antecedent basis. Pursuant to claim 52, at end of step c) insert a semicolon in place of a comma. Pursuant to claim 54, at end of step b), insert a semicolon in place of a comma. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Rejection of claims 28, 30-52 and 54

4. Claims 28, 30-52 and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Scepanovic et al., U.S. Patent 5,699,265.

5. Pursuant to claim 28, Scepanovic '625 discloses a placer that places circuit modules in integrated circuit layouts, the placer using a set of partitioning lines, that define a plurality of slots, to partition an IC layout region into a plurality of sub-regions corresponding to said slots (col. 3, ll. 10-19, ll. 34-37), a method of pre-computing costs of placing circuit modules in an IC layout region (col. 3, ll. 20-23), the method comprising a) selecting a first group of said slots (col. 5, ll. 7-22); b) computing a first attribute of a set of one or more interconnect lines necessary for connecting the first group of said slots, wherein computing the first attribute comprises calculating the length of said set of interconnect lines (col. 6, ll. 16-21); c) computing a second attribute of the set of interconnect lines (col. 8, ll. 3-9); and d) storing the computed attributes in a storage structure (fig. 2, #38; col. 4, ll. 60-67).

6. Pursuant to claim 30, wherein computing the second attribute comprises calculating number of bends in said set of interconnect lines (col. 8, ll. 3-9).

7. Pursuant to claim 31, wherein the bends are diagonal bends (Fig. 9).

8. Pursuant to claim 32, wherein a plurality of line paths exist between said slots, wherein computing the first attribute comprises identifying the line paths used by said set of interconnect lines (Fig. 8).

9. Pursuant to claim 33, wherein a plurality of edges exist between said slots, wherein computing the first attribute comprises identifying the edges intersected by said set of interconnect lines (Fig. 8, col. 8, line 65 to col. 9, line 4).

10. Pursuant to claim 34, further comprising computing a third attribute of the set of interconnect lines; and storing the computed third attribute in the storage structure (col. 8, ll. 30-57, the median).

11. Pursuant to claim 35, further comprising selecting a second group of said slots different from said first group; computing first and second attributes of a set of one or more interconnect lines connecting the second group of said slots; storing the computed attributes in the storage structure (col. 5, ll. 16-44).

12. Pursuant to claim 36, Scepanovic '625 discloses a method of pre-computing costs of placing circuit elements within an integrated circuit layout (col. 3, ll. 20-23) comprising defining a partitioning grid having a plurality of slots, said partitioning grid for partitioning a region of an IC layout during a placement operation (col. 3, ll. 20-23); for each combination of said slots, defining at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of said slots (col. 6, ll. 16-32); computing multiple attributes for each of said connection graphs (col. 6, ll. 16-21; col. 8, ll. 3-9); storing the computed attributes in a storage structure (fig. 2, #38; col. 4, ll. 60-67).

13. Pursuant to claim 37, wherein the connection graphs are Steiner trees (col. 8, ll. 50-64).

14. Pursuant to claim 38, wherein the connection graphs are minimum spanning trees (col. 7, ll. 1-31).

15. Pursuant to claim 39, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph (Fig. 8, 9, col. 8, line 50 to col. 9, line 6).

16. Pursuant to claim 40, wherein computing multiple attributes of each connection graph comprises calculating the number of bends in each graph (col. 8, ll. 3-9).

17. Pursuant to claim 41, wherein the bends are diagonal bends (Fig. 9).

18. Pursuant to claim 42, wherein the partitioning grid has a plurality of edges between said slots (col. 5, line 25 to col. 6, line 25) and wherein computing multiple attributes of each connection graph comprises identifying the edges intersected by each graph (col. 8, line 3 to col. 10, line 4).

19. Pursuant to claim 43, wherein said partitioning grid having a particular structure (col.5, ll. 7-23), wherein said edges are defined based on a wiring model for the IC layout and on the structure of the partitioning grid (col. 5, line 7 to col. 6, line 25).

20. Pursuant to claim 44, wherein the partitioning grid having a plurality of interconnect line paths between said slots, wherein computing multiple attributes of each connection graph comprises identifying the paths used by each graph (Fig. 8, 10a, 10b illustrates this limitation).

21. Pursuant to claim 45, wherein said partitioning grid having a particular structure, wherein said interconnect line paths are defined based on a wiring model for the IC layout and on the structure of the partitioning grid (col. 5, line 7 to col. 6, line 25).

22. Pursuant to claim 46, wherein the partitioning grid having a plurality of interconnect line paths between said slots, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph and identifying the paths used by each graph (col. 8, line 59 to col. 9, line 28).

23. Pursuant to claim 47, wherein the partitioning grid having a plurality of edges between said slots, wherein computing multiple multiple attributes of each connection graph comprises calculating the length of each graph and identifying the edges used by each graph (col. 8, line 59 to col. 9, line 28).

24. Pursuant to claim 48, wherein the partitioning grid is formed by a set of partitioning lines (Fig. 4; col. 5, ll. 16-37).

25. Pursuant to claim 49, wherein the partitioning lines are horizontal and vertical lines (Fig. 4).

26. Pursuant to claim 50, which recites a method of pre-computing costs of placing circuit elements (col. 3, ll. 20-23), the method comprising defining a partitioning grid having a plurality of slots, said partitioning grid for partitioning a region of an IC layout into a plurality of sub-regions corresponding to said slots (col. 3, ll. 11-37); for each combination of said slots, identifying at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of said slots; computing the length and number of bends in each of said connection graphs (col. 6, ll. 16-50); for each particular combination of said slots, storing the length of a connection graph identified for that particular combination of said slots, wherein when more than one connection graph is defined for that particular combination of said slots (col. 8, ll.

59-64), the method storing the length of shortest connection graph that has less than a predetermined number of bends (col. 10, ll. 45-65).

27. Pursuant to claim 51, further comprising for each particular combination of said slots that has more than one identified connection graph, storing the length of shortest connection graph that has less than a second predetermined number of bends, when none of the connection graphs for the particular combination of slots have less than the first predetermined number of bends. (col. 11, line 62 to col. 14, line 34).

28. Pursuant to claim 52, Scepanovic discloses a method of placing circuit modules in a region of an integrated circuit (col. 4, ll. 57-60), the method comprising partitioning the IC region into several sub-regions (Figs. 5, 6); selecting a net (col. 6, ll. 26-32); identifying the set of sub-regions containing the circuit elements of the selected net (col. 8, ll. 10-49); retrieving from a storage structure multiple pre-computed attributes of a set of one or more interconnect lines necessary for connecting the identified set of sub-regions (col. 8, line 3 to col. 9, line 4); computing a placement cost of said net within said region by using the retrieved attributes (col. 8, line 3 to col. 9, line 4); changing the position of a circuit element of the net from one sub-region to another (Fig. 7, divide set of cells; modify region sizes); identifying a new set of sub-regions that contain the circuit elements of the net (Fig. 7, modify region sizes); retrieving multiple pre-computed attributed of a different set of interconnect lines necessary for connecting the identified new set of sub-regions; and computing a new placement cost of said net within said region by using the attributes retrieved for the different set of interconnect lines (col. 9, ll. 47-65).

29. Pursuant to claim 54 Scepanovic teaches a method comprising: partitioning the IC layout region into several sub-regions (Figs. 5, 6); for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net (col. 8, ll. 10-49); for each particular net, retrieving multiple pre-computed attributes of a connection graph that models the topology of interconnect lines needed to connect the identified set of sub-regions of the particular net, wherein the connection graph is either a Steiner tree or a minimum spanning tree (col. 8, ll. 3-64); computing a placement cost for the IC layout within said region by using the retrieved attributes (col. 9, ll. 41-67).

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing.

31. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

32. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

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